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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,005	06/14/2001	Michio Horiuchi	149-01	5592

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EXAMINER
COSTANZO, PATRICIA M

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/881,005	HORIUCHI ET AL.	
	Examiner	Art Unit	
	Patricia M. Costanzo	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18* is/are pending in the application.

4a) Of the above claim(s) *6 - 10, 17, and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 5 and 11 - 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 1 – 5 and 11 – 13, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent No. 6,335,565 (Miyamoto *et al.*). The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Referring to Claim 1: Miyamoto *et al.* disclose a multi-layered semiconductor device (see multi-layer device in Figure 34 in conjunction with Col. 6, line 4 - 12) characterized in that a semiconductor package (Col. 6, line 6) incorporating therein a semiconductor chip (Figure 34, (AD) and (MF) is disposed in a package accommodation opening (Figure 34 (3b)) (see Col. 27, lines 5 – 15) to form a circuit board, and a plurality of such circuit boards are layered together to electrically connect circuit patterns of the respective circuit boards with each other (Col. 38. line 37 – 47).

Miyamoto *et al.* do not specifically disclose a film-like semiconductor package.

However, Miyamoto *et al.* do specifically disclose that each of the tape carriers is made of a material such as polyimide film (Col. 26, lines 33 – 34), thus it is obvious that the semiconductor package is film-like.

Miyamoto *et al.* do not specifically disclose a circuit pattern layer, but see Col. 27, line 5 – 15, for the teaching of etching (patterning) of the copper foil to form leads and holes, which obviously creates a circuit pattern layer.

Referring to Claim 2: The proposed device of Miyamoto *et al.* discloses a multi-layered semiconductor device, as recited above, further disclosing wherein every adjacent circuit board is bonded to another with an insulation adhesive except for an electrically connected portion (see, Figure 34, adhesive (10), Col.22, lines 39 – 42, and Col. 26, lines 38 - 39).

Referring to Claim 3: The proposed device of Miyamoto *et al.* discloses a multi-layered semiconductor device, as recited above, further disclosing wherein the electrical connection between the circuit patterns on the respective circuit boards is performed via a low melting point metal filled in a through-hole formed in the semiconductor package or the circuit board (see, Figure 34, (11) and Col. 26, lines 41 - 44).

Referring to Claim 4: The proposed device of Miyamoto *et al.* discloses a multi-layered semiconductor device, as recited above, further disclosing wherein the electrical connection between the circuit patterns on the respective circuit boards is performed by connecting an extension of the circuit pattern into a hole formed in the semiconductor package or the circuit board with an electrode pad of the circuit pattern in the other circuit board positioned beneath the former circuit

board (see, Figure 34, solder (11) connecting copper leads (5a) and bumps (9), in conjunction with Col.27, lines 9 –20).

Referring to Claims 5: The proposed device of Miyamoto *et al.* discloses a multi-layered semiconductor device, as recited above, further disclosing wherein the electric connection between the semiconductor package and a circuit pattern layer accommodating the semiconductor package is performed by connecting an extension of the circuit pattern, formed on the semiconductor package to project outside the package with an electrode pad of the circuit pattern layer (see, Figure 34, bump (9)).

Referring to Claim 11: The proposed device of Miyamoto *et al.* discloses a multi-layered semiconductor device, as recited above, further disclosing an insulation substrate (note: polyimide makes an insulating substrate) (see, Col. 26, line 33 - 34).

Referring to Claim 12: The proposed device of Miyamoto *et al.* discloses a multi-layered semiconductor device, as recited above, further disclosing wherein at least one of the plurality of circuit boards incorporates a plurality of semiconductor chip therein (see, Col. 6, lines 4 - 7).

Referring to Claims 13 and 16: The proposed device of Miyamoto *et al.* discloses a multi-layered semiconductor device, as recited above, including the limitations recited by Claim 13.

Referring to Claims 15: The proposed device of Miyamoto *et al.* discloses a multi-layered semiconductor device, as recited above, further disclosing wherein the electric connection between the semiconductor chip and the board is by a flip-chip connection (see, Figure 34, bumps (4)).

2. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent No. 6,335,565 (Miyamoto *et al.*) in view of United States Patent Application Publication No. US 2001/0001989 (Smith) Application No. 09/757,897.

The proposed device of Miyamoto *et al.* discloses a multi-layered semiconductor device, as recited above, except for disclosing wherein the semiconductor chip is electrically connected to the circuit of the circuit board by a beam lead bonding.

Smith discloses the use of beam leads to electrically connect a chip to a circuit board (see, Figure 21 (12) in conjunction with [0092] lines 8 – 9 and [0093] lines 5 – 11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device disclosed by Miyamoto *et al.* by providing for the use of beam leads to electrically connect a chip to a circuit board as disclosed by Smith as it was well known to use beam leads to connect a chip to a substrate and to obtain the advantage of having the lead project outwardly away from the chip ([0092] lines 8 - 9) to accommodate a substrate that is located at a lateral distance from the chip, for example.

Conclusion

Any inquiry concerning this communication should be directed to Patricia Costanzo at 703 305 5675 on Monday – Friday from 8:00 A.M. – 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful Supervisory Primary Examiner Tom Thomas can be reached at 703 308 2772.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist at 703 308 0956.

Using facsimile machines to transmit correspondence is encouraged.

Papers may be faxed directly to Examiner at 703 745 2002.

The official Technical Center 2800 before-final FAX number is 703 872 9318 and the after-final FAX number is 703 872 9319. These FAX numbers will provide the FAX sender with an auto-reply verifying receipt of their FAX by the United States Patent and Trademark Office. If there should be a problem while faxing to the Office, please contact Technical Center 2800 Customer Service at 703 306 3329.

pmc
July 1, 2002

Steven Loke
Primary Examiner

Steven Loke